THAT WHICH IS CLAIMED IS:

1. An integrated circuit memory device, comprising:

a memory array having a page of multi-port memory cells therein that spans at least X columns and Y rows, said page configured to support writing and reading of first data vectors to and from the X columns and writing and reading of second data vectors to and from the Y rows, where X and Y are unequal integers.

2. The memory device of Claim 1, wherein the first data vectors are Y-bit words; and wherein the second data vectors are X-bit words.

3. The memory device of Claim 2, wherein Y=72 and X=36.

4. The memory device of Claim 1, wherein the multi-port memory cells are quad-port memory cells.

5. The memory device of Claim 1, further comprising:

a check bit generation circuit that is configured to receive outgoing second data vectors from said memory array; and

an error detection and correction circuit that is configured to provide incoming second data vectors to said memory array.

6. A first-in first-out (FIFO) memory device, comprising:

a first cache memory device having a first page of quad-port memory cells therein that is configured to support writing and reading of FIFO vectors to and from columns in the first page and writing and reading of memory vectors to and from rows in the first page.

7. The memory device of Claim 6, further comprising a second cache memory device that is configured to operate in tandem with said first quad-port cache memory device so that FIFO write operations periodically switch back-and-forth between said first cache memory device and said second cache memory device.

8. The memory device of Claim 6, wherein each of the memory vectors includes one bit of data from each of the FIFO vectors and vice versa.

9. The memory device of Claim 6, further comprising:

a check bit generation circuit that is configured to receive outgoing FIFO vectors from said first cache memory device; and

an error detection and correction circuit that is configured to provide incoming memory vectors to said first cache memory device.

10. An integrated circuit memory device, comprising:

a memory array having a page of quad-port memory cells therein that spans at least X columns and Y rows, said page configured to support writing and reading of first data vectors having widths equal to Y-bits and writing and reading of second data vectors having widths equal to X-bits, where X and Y are unequal integers.

11. The memory device of Claim 10, wherein the first data vectors are written to and read from columns of said page; and wherein the second data vectors are written to and read from rows of said page.

12. The memory device of Claim 11, wherein the first data vectors are FIFO data vectors; and wherein the second data vectors are RAM-compatible data vectors.

13. The memory device of Claim 12, wherein Y=72 and X=36.

14. The memory device of Claim 11, further comprising:

a check bit generation circuit that is configured to receive outgoing second data vectors from said memory array; and

an error detection and correction circuit that is configured to provide incoming second data vectors to said memory array.

15. A method of operating an integrated circuit memory device having first and second buses therein with unequal widths, comprising the steps of:

writing a page of data by transferring a plurality of first data vectors from the first bus to a respective plurality of columns of multi-port memory cells within a memory array; and

reading the page of data by transferring a plurality of second data vectors from respective rows of the memory array to the second bus.

16. The method of Claim 15, wherein each of the plurality of second data vectors includes a data bit from each of the plurality of first data vectors and vice versa.

17. The method of Claim 15, wherein the memory device is a FIFO memory device.

18. A method of operating a first-in first-out (FIFO) memory device, comprising the steps of:

writing a page of data into the FIFO memory device by transferring a first plurality of FIFO data vectors into a respective plurality of columns of multi-port memory cells within a first cache memory array; and

copying the page of data from the first cache memory array into an embedded or external RAM array by transferring a plurality of memory data vectors from respective rows of the first cache memory array to the RAM array.

19. The method of Claim 18, wherein each of the plurality of memory data vectors includes a respective data bit from each of the plurality of FIFO data vectors.

20. The method of Claim 18, further comprising the steps of:

transferring the page of data from the RAM array into a second cache memory array within the FIFO memory device; and

reading the page of data from the second cache memory array by sequentially transferring a second plurality of FIFO data vectors from respective columns of multi-port memory cells within the second cache memory array to an output data bus.

21. The method of Claim 20, wherein the step of transferring the page of data from the RAM array into the second cache memory array comprises writing a plurality of memory data vectors into rows of the second cache memory array.

22. A first-in first-out (FIFO) memory device, comprising:

a multi-port cache memory device having a write port that is configured to receive write data during FIFO write operations and a read port that is configured to supply read data during FIFO read operations;

a supplemental memory device that is configured to retain next-to-read FIFO data that was previously written into said multi-port cache memory device; and

a data transfer control circuit that is configured to provide said multi-port cache memory device with a copy of the next-to-read FIFO data that is error checked and corrected during memory-to-cache read operations that hide error correcting latency from the FIFO read operations.

23. The FIFO memory device of Claim 22, wherein said multi-port cache memory device comprises at least first and second quad-port memory devices; and wherein said data transfer control circuit comprises a first error checking and correction circuit that is coupled to said first quad-port memory device and a second error checking and correction circuit that is coupled to said second quad-port memory device.

24. The FIFO memory device of Claim 22, wherein said multi-port cache memory device and said supplemental memory device are on first and second semiconductor chips, respectively.

25. The FIFO memory device of Claim 24, wherein said supplemental memory device is a random access memory (RAM) device.

26. The FIFO memory device of Claim 23, wherein said data transfer control circuit further comprises a first check bit generation circuit that is coupled to said first quad-port memory device and a second check bit generation circuit that is coupled to said second quad-port memory device.

27. The FIFO memory device of Claim 23, wherein said first quad-port memory device has a first page of quad-port memory cells therein that is configured to support writing and reading of FIFO vectors to and from columns in the first page and writing and reading of memory vectors to and from rows in the first page.

28. A FIFO controller having a unidirectional data input port, a unidirectional data output port and a bidirectional data port, said FIFO controller comprising:

a check bit generation circuit having an output electrically coupled to the bidirectional data port;

an error detection and correction circuit having an input electrically coupled to the bidirectional data port; and

a quad-port data cache having a first port that is configured to accept FIFO write data received by the unidirectional data input port, a second port that is electrically coupled to an input of said check bit generation circuit, a third port that is electrically coupled to an output of said error detection and correction circuit and a fourth port that is configured to pass FIFO read data to the unidirectional data output port.

29. A FIFO controller having a unidirectional data input port, a unidirectional data output port and a bidirectional data port, said FIFO controller comprising:

a first check bit generation circuit having an output electrically coupled to the bidirectional data port;

a first error detection and correction circuit having an input electrically coupled to the bidirectional data port;

a second check bit generation circuit having an output electrically coupled to the bidirectional data port;

a second error detection and correction circuit having an input electrically coupled to the bidirectional data port;

a first quad-port cache having a first port that is configured to accept FIFO write data received by the unidirectional data input port, a second port that is electrically coupled to an input of said first check bit generation circuit, a third port that is electrically coupled to an output of said first error detection and correction circuit and a fourth port;

a second quad-port cache having a first port that is configured to accept FIFO write data received by the unidirectional data input port, a second port that is electrically coupled to an input of said second check bit generation circuit, a third port that is electrically coupled to an output of said second error detection and correction circuit and a fourth port; and

a quad-port cache control circuit that is configured to hide error detection and correction latency in a read data path by passing FIFO read data from the fourth ports of said first and second quad-port caches to the unidirectional data output port in a back and forth manner.

30. An integrated circuit device having a FIFO read port and a FIFO write port and comprising:

a FIFO controller that is configured as an interface between the FIFO read and write ports and a high capacity random access memory (RAM) device located external to the integrated circuit device, said FIFO controller comprising:

an error detection and correction circuit disposed in a read data path between the RAM device and the FIFO read port;

at least first and second quad-port cache devices; and

a control circuit electrically coupled to said error detection and correction circuit and said at least first and second quad-port cache devices, said control circuit configured to operate said at least first and second quad-port cache devices in a manner that hides error detection and correction latency in the read data path during read operations from the FIFO read port.

31. An integrated circuit device having a FIFO read port and a FIFO write port and comprising:

a FIFO controller that is configured as an interface between the FIFO read and write ports and a high capacity random access memory (RAM) device, said FIFO controller comprising:

an error detection and correction circuit disposed in a read data path between the RAM device and the FIFO read port;

at least first and second quad-port cache devices; and

a control circuit electrically coupled to said error detection and correction circuit and said at least first and second quad-port cache devices, said control circuit configured to operate said at least first and second quad-port cache devices in a manner that hides error detection and correction latency in the read data path during read operations from the FIFO read port.

32. An integrated circuit memory device, comprising:

first and second memory devices that are electrically coupled together by a first data path that is configured to transfer write data from said first memory device to said second memory device when said first memory device is undergoing write operations and a second data path that is configured to transfer read data from said second memory device to said first memory device when said first memory device is undergoing read operations; and

an error correction circuit that is configured to check and correct read data in the second data path using operations that hide error correcting latency from the read operations.

33. A method of operating a first-in first-out (FIFO) memory device having a cache memory device therein that comprises a plurality of multi-port memory devices, said method comprising the steps of:

reading a current page of data from one of the plurality of multi-port memory devices while simultaneously arbitrating to determine whether or not the cache memory device retains all next-to-read data relative to the current page of data; and

then, in response to determining that the cache memory device does not retain all next-to-read data relative to the current page of data, transferring a next-to-read page of data, which has been error-checked and error-corrected, from a non-cache memory device into the cache memory device.

34. The method of Claim 33, wherein said transferring step is followed by the steps of:

reading an error-checked page of data from another one of the plurality of multi-port memory devices while simultaneously arbitrating to determine whether or not the cache memory device retains all next-to-read data relative to the error-checked page of data; and

then, in response to determining that the cache memory device retains all next-to-read data relative to the error-checked page of data, reading data that has not been error-checked from the cache memory device.

35. A signal arbitration method, comprising the steps of:

arbitrating between first and second request signals generated in respective first and second clock domains that are asynchronously timed relative to each other, to obtain first arbitration results that identify a relative queue priority between the first and second request signals; and

transferring the first arbitration results into a third clock domain that is asynchronously timed relative to the first and second clock domains.

36. The method of Claim 35, wherein said transferring step comprises:

arbitrating the first arbitration results in a third clock domain to obtain second arbitration results that confirm or correct the first arbitration results.

37. The method of Claim 36, wherein said step of arbitrating the first arbitration results is followed by the step of arbitrating the second arbitration results in the third clock domain to obtain third arbitration results that confirm or correct the second arbitration results.

38. The method of Claim 35, wherein the first and second request signals are read and write request signals, respectively.

39. A signal arbitration method, comprising the steps of:

arbitrating between first and second request signals generated in respective first and second clock domains that are asynchronously timed relative to each other, to obtain intermediate arbitration results that identify a relative queue priority between the first and second request signals; and

arbitrating between a third request signal and the intermediate arbitration results in a third clock domain that is asynchronously timed relative to the first and second clock domains, to obtain final arbitration results that identify a relative queue priority between the first, second and third request signals.

40. The method of Claim 39, wherein the third request signal has a higher request priority relative to the first and second request signals.

41. The method of Claim 40, wherein the first, second and third request signals are received in a first-then-second-then-third timing sequence; and wherein said step of arbitrating between the first and second request signals is followed by the step of performing operations associated with the first, second and third requests one-at-a-time in a first-then-third-then-second operation sequence.

42. The method of Claim 40, wherein the first, second and third request signals are received in a second-then-first-then-third timing sequence; and wherein said step of arbitrating between the first and second request signals is followed by the step of performing operations associated with the first, second and third requests one-at-a-time in a second-then-third-then-first operation sequence.

43. A signal arbitration method, comprising the steps of:

arbitrating between first and second request signals generated in respective first and second clock domains that are asynchronously timed relative to each other, to obtain first arbitration results that identify the first request signal as having a higher queue priority relative to the second request signal;

transferring the first arbitration results into a third clock domain that is asynchronously timed relative to the first and second clock domains;

issuing a first start command corresponding to the first request signal in the third clock domain, while maintaining the second request signal as a queued second request; and

arbitrating between a third request signal and the queued second request to obtain second arbitration results that identify a relative queue priority between the second queued request and the third request signal.

44. The method of Claim 43, wherein the second arbitration results identify the third request signal as having a higher queue priority relative to the second queued request when said step of arbitrating between a third request signal and the queued second request occurs prior to completion of operations responsive to the first start command.

45. A signal arbitration method, comprising the steps of:

evaluating read and write request signals to detect a read-then-write or write-then-read timing order therebetween;

issuing a read start command corresponding to the read request signal in response to detecting the read-then-write timing order, while maintaining the write request signal as a queued write request;

evaluating a refresh request signal to detect a presence or an absence of a timing overlap between a refresh request and operations associated with the read start command; and then

issuing a refresh start command while the write request remains queued pending completion of operations associated with the refresh start command, in response to detecting the presence of a timing overlap.

46. A method of arbitrating between at least three request signals, comprising the steps of:

evaluating at least first and second request signals having first and second request priorities, respectively, to detect a first-then-second or second-then-first timing order therebetween;

issuing a first start command corresponding to the first request signal in response to detecting the first-then-second timing order, while maintaining the second request signal as a queued second request;

evaluating a third request signal having a higher request priority relative to the second request priority to detect a presence or an absence of a timing overlap between the third request and operations associated with the first start command; and then

issuing either a second start command corresponding to the queued second request in response to detecting the absence of a timing overlap, or a third start command corresponding to the third request in response to detecting the presence of a timing overlap.

47. A signal arbitration device, comprising:

a multi-stage arbitration control circuit that is configured to arbitrate between at least first and second request signals generated in respective first and second clock domains that are asynchronously timed relative to each other and transfer arbitration results that identify a relative queue priority between the first and second request signals into a third clock domain that is asynchronously timed relative to the first and second clock domains.

48. The device of Claim 47, wherein said multi-stage arbitration control circuit comprises:

a first arbitration stage that is configured to arbitrate a request priority between the at least first and second request signals and generate first arbitration results that identify a relative queue priority between the at least first and second request signals; and

a second arbitration stage that is configured to buffer and rearbitrate a request priority associated with the first arbitration results.

49. The device of Claim 48, wherein said second arbitration stage is responsive to a clock signal that operates in the third clock domain.

50. The device of Claim 48, wherein said multi-stage arbitration control circuit is configured to double buffer the first arbitration results.

51. The device of Claim 50, wherein said second arbitration stage is configured to generate second arbitration results that confirm or correct the first arbitration results.

52. The device of Claim 51, wherein said multi-stage arbitration control circuit further comprises:

a third arbitration stage that is configured to buffer and rearbitrate a request priority associated with the second arbitration results.

53. The device of Claim 52, wherein said third arbitration stage is electrically coupled to a clock control circuit that is responsive to the third arbitration results.

54. The device of Claim 53, wherein the clock control circuit is responsive to the clock signal that operates in the third clock domain.

55. A signal arbitration device, comprising:

a multi-stage arbitration control circuit that is configured to arbitrate between read and write request signals generated in respective first and second clock domains that are asynchronously timed relative to each other and is further configured to transfer arbitration results that identify a relative queue priority between the read and write request signals into a third clock domain that is synchronously timed relative to the first and second clock domains; and

a refresh command buffer and arbitration circuit that is responsive to a refresh start command and read and write start signals generated by said multi-stage arbitration control circuit.

56. The device of Claim 55, further comprising a clock control circuit that is responsive to read, write and refresh start signals generated by said multi-stage arbitration control circuit and said refresh command buffer and arbitration circuit.

57. The device of Claim 56, wherein said multi-stage arbitration control circuit is responsive to a clock signal generated by said clock control circuit.

58. The device of Claim 57, wherein said multi-stage arbitration control circuit comprises a third stage that is synchronized with the clock signal generated by said clock control circuit.

59. A method of operating a FIFO memory device, comprising the steps of:

writing a plurality of FIFO vectors into a cache memory device; and

transferring at least one memory vector from the cache memory device to a row within a supplemental memory device during a cache-to-memory data transfer operation, said at least one memory vector comprising at least one bit from each of the plurality of FIFO vectors.